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SYNTHESIS OF DIGITAL RADIO RECEIVER SYSTEM FOR SECURE COMMUNICATION WITH FREQUENCY-HOPPING SPREAD SPECTRUM

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Summary. *It was represented the results of synthesis and modeling of work of digital receiver based on the digital down converter (DDC), and a digital signal processor (DSP), which are used to process received signals. The method of constructing narrow-band receiver with digital filtering, demodulation and signal processing, the results of its use in digital radio with frequency-hopping spread spectrum (FHSS mode) is discussed.*

Key words: *Frequency-hopping spread spectrum (FHSS mode), Digital receiver signal processor DSP, Digital Down Converter (DDC), quadrature demodulator, frequency modulation (FM).*

Introduction. Problem Research. Intensive development of telecommunication systems in recent decades makes difficulties in constructing new information with radio access networks. Electromagnetic radio channels conditions in all frequency ranges up to millimeter become more difficult, so new radio devices have to work in intensive influence of external random, and in some cases, malicious interferences. Reduction of the reliability of received data as a result of these factors is a major obstacle to providing quality communication.

Particularly acute issue is for radio systems designed to transfer sensitive or confidential information, which often work in close proximity with many existing radio equipment for various purposes. First at all, this applies to military radio communication systems, radio dispatch communication on transport, radio transmission of banking information, LANs equipment for medical systems, radio informing systems of population of Ministry of Emergency Services and many others.

Generally, the synthesis of radio device architecture, the choice of the methods of signal processing for subscribers information exchange, methods for best access to subscriber, information transfer speed, reliable data protection from unauthorized access in conditions of influence of interference is an urgent task and require additional researches, especially to make a method for choosing the right and optimal parameters of digital connection channel to create a multi-channel communication systems with abrupt changing of operating frequency.

Analysis of the research according to topics. Digital frequency down converter is as alternative for the architecture of superheterodyne receiver, especially with high integration level and low power consumption. The research on the use of digital down converter is shown at [1 – 4]. Their fundamental advantage isflexebility of channel parameters tuning.

Digital frequency abridger is commonly used in the design of digital receivers based on broadband multiple access with code distribution of channels WCDMA (Wideband Code Division Multiple Access) and using mobile implementation CDMA2000 [5, 6]. In mentioned publications are not covered synthesis methods, configuring and checking parameters of radio channels, including narrowband communication systems with FHSS for VHF frequency. For the purpose of efficient synthesis of such digital radios for narrowband communication systems it is useful to have an adequate model for the study and channel settings without the need for costly prototyping or implementation of the radio station.

Analysis and synthesis of the channel using a digital frequency converter

To ensure reasonable reliability of the transmission of information in communication systems, we use special, more difficult and costly methods and tools, such as: increasing the transmitter power, the use of frequency diversity transmission, mixing information (scrambling), the introduction of information flow redundant information with application of noise-immunity error correction coding, etc.

Many modern radio architectures have comprising down conversion that convert high-frequency (HF) or ultra-high frequency (UHF) level to a lower intermediate frequency for use in the main frequency band. Depending on the application (as for example, aerospace, defense industry, commercial communication), communication systems work in the HF and UHF frequency bands. A common solution for receivers is to use a larger number of conversions and decrease in filtration rate. For these tasks more efficient modern solution is to use radio frequency (RF), ADC with Digital Down Converter (DDC) and signal processor DSP or programmable logic integrated circuits (FPGA) for demodulation of input signal.

The ability of high-speed ADC for processing a range of hundreds of MHz frequency bands allows avoiding the use of intermediate frequencies at the analog part. The inclusion of integrated DDC allows performing transfer spectrum in lower frequency region while providing greater bandwidth through ADC with high sampling frequency and perform filtering and decimation signal. This solution provides the advantage by increasing the dynamic range within the frequency band (increases SNR), and decreases frequency for further processing using signal processor DSP or programmed logic arrays FPGA.

Synthesis of digital radio channel models

For choosing and researching the parameters of modeling of the communication channel (Fig. 1) is prepared with the package of Multisim, for this purpose, we use a with low frequency signal generator (sin), frequency modulator (FM Modulator Passband), a block of channel model (channel, Fig. 2), the DDC block AD6620, the demodulator block (Demod) and low frequency filter (RxDemod).
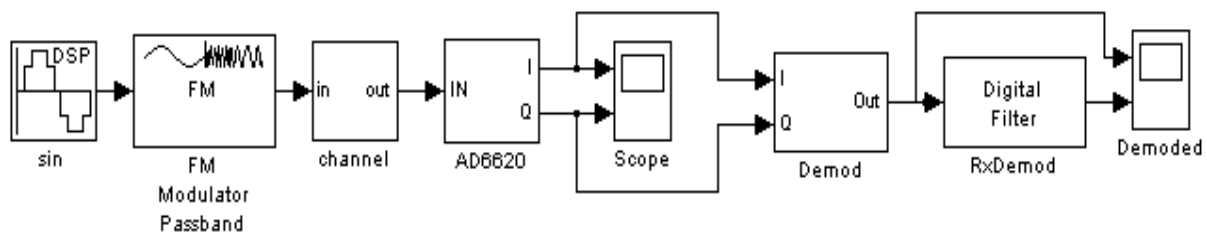

Figure 1. Model of communication channel

The communication channel is modeled with bandwidth limitations and superposition of additive Gaussian noise. A block of saturation models the use of the automatic gain control at a channel receiver.
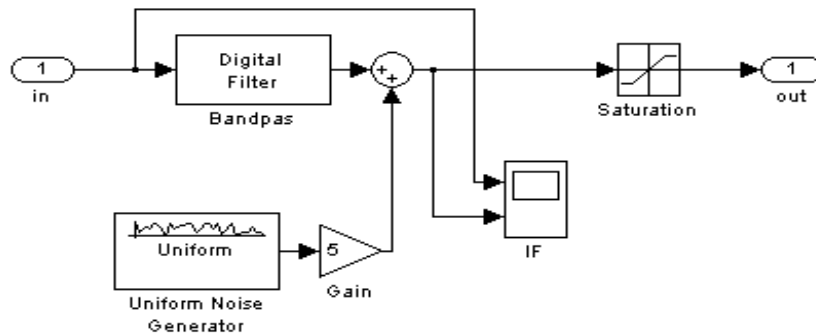

Figure 2. Model of signal distribution channel

Simulation modeling of the digital converter AD6620

The principle of DDC AD6620 is based on quadrature signal processing, where the input signal is multiplied by two basic frequency shifted in phase by 90° [7], according to the formulas 1 – 2.

$$y_I(t) = s(t)cos\omega_0 t = Acos(\omega_0 t + \varphi(t))cos\omega_0 t$$
$$y_I(t) = \frac{A}{2}cos\varphi(t) + \frac{A}{2}cos(2\omega_0 t + \varphi(t))$$
(1)

$$y_Q(t) = s(t)sin\omega_0 t = Acos(\omega_0 t + \varphi(t))sin\omega_0 t$$
$$y_Q(t)\frac{A}{2}sin\varphi(t) + \frac{A}{2}sin(2\omega_0 t + \varphi(t))$$
(2)

As a result of multiplying the receive signals I and Q, from which after filtering and processing of quadrature demodulator, the original signal is extracted.

The scheme DDC AD6620 consists of controlled digital generator NCO, two mixers and filters CIC2, CIC5 and FIR (Fig. 3). Software-controlled generator heterodyning NCO of the reference frequency forms two harmonic signals shifted in phase by 90 °. The input digital signal on two mixers is multiplied parallel by the NCO generator signals and as a result signals I and Q are shaped, which are filtered and decimated at CIC-filters (Cascaded Integrator-Comb) of second and fifth orders. CIC filter does not require multiplication operations and can significantly reduce the sampling rate that decreases hardware and computing resources. Increasing of filter order in one can reduce the level of side lobes to 11..13 dB. So if CIC filter frequency is uneven, then for adjusting it in a bandwidth is used FIR – filter (Finite Impulse Response), which provides linearity in the passband and high selectivity of the signal, graphic of output signals I and Q shown on Fig. 4. The filtered and decimated signals are processed with quadrature demodulator and LF filter.
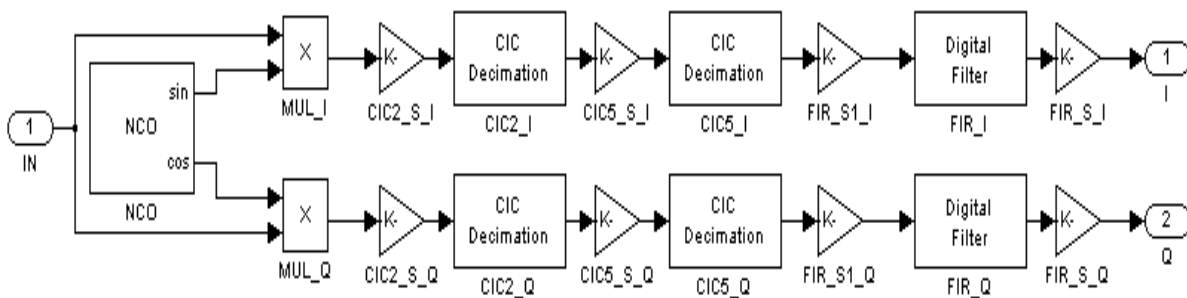

Figure 3. Functional scheme of digital convertor DDC AD6620

It is important to ensure quality narrowband filter signals to ensure a high level of channel selectivity, to avoid interference and noise exposure.
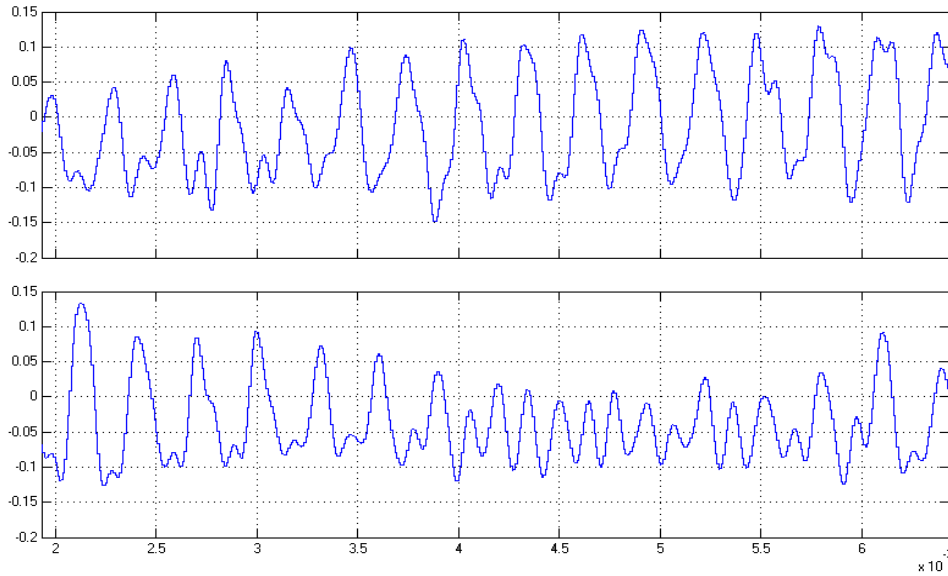
Figure 4. Graphics of signals I and Q at output DDC AD6620

Calculation of filters for DCC and convertor AD6620

To calculate filters, a software package from Analog device SoftCell FilterDesign is used. Channel options for calculating the following system: input frequency 10.7 MHz, output frequency of 80 kHz, sampling frequency 25.6 MHz, bandwidth 7.5 kHz. From estimated coefficients are selected the following parameters (Fig. 5) RCF = 1, CIC5 = 32, CIC2 = 10 frequency cut-off of the filter – 12.5 kHz and signal weakening – -70dB. Filters frequency responses are plotted in the Filter Visualization Tool – MATLAB & Simulink. Frequency responses of CIC filters of second (f) and fifth order (b) are shown on the figure 6, and of the FIR filter is shown on the Figure 7.
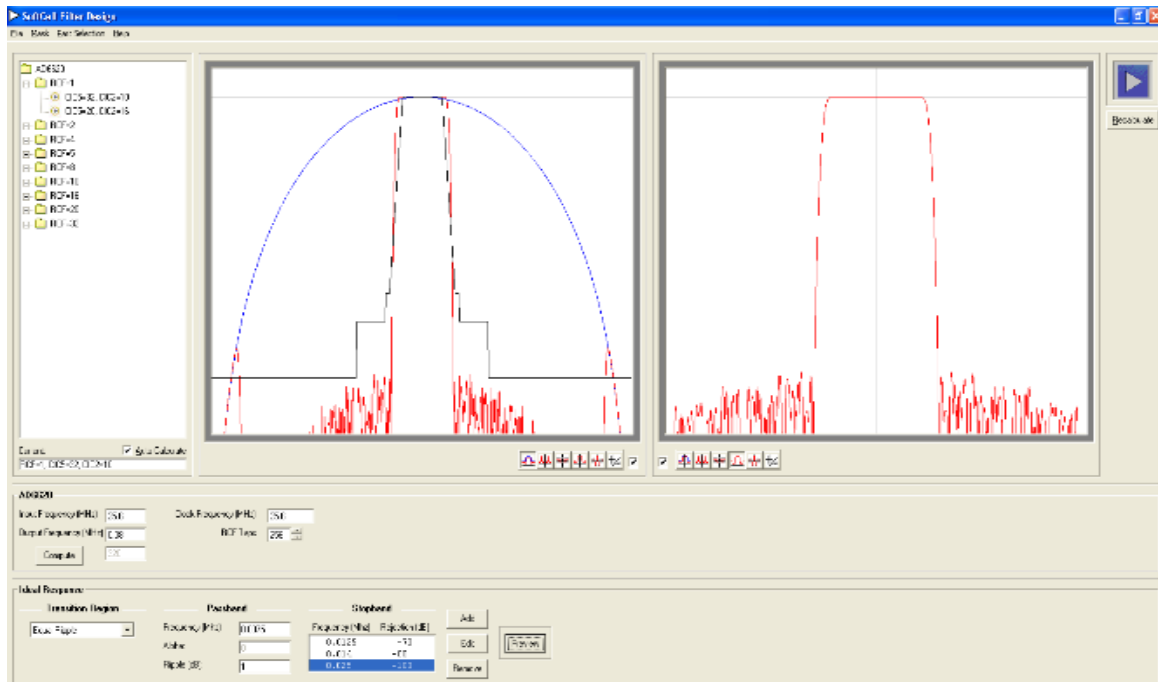

Figure 5. Graphic of the filter DDC AD6620 at program package SoftCell FilterDesign
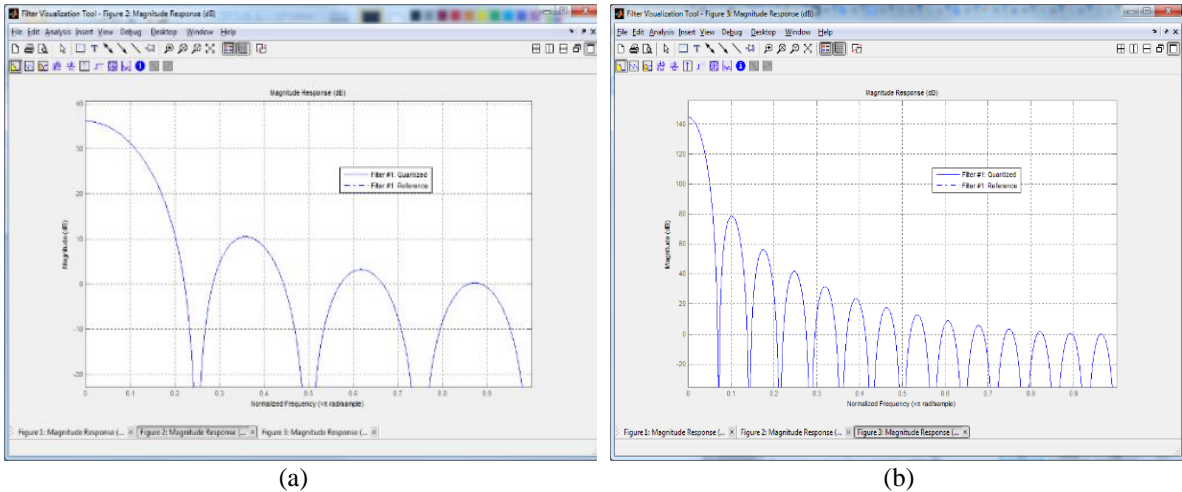
Figure 6. Graphic of CIC filters of second order (a) and fifth order (b)
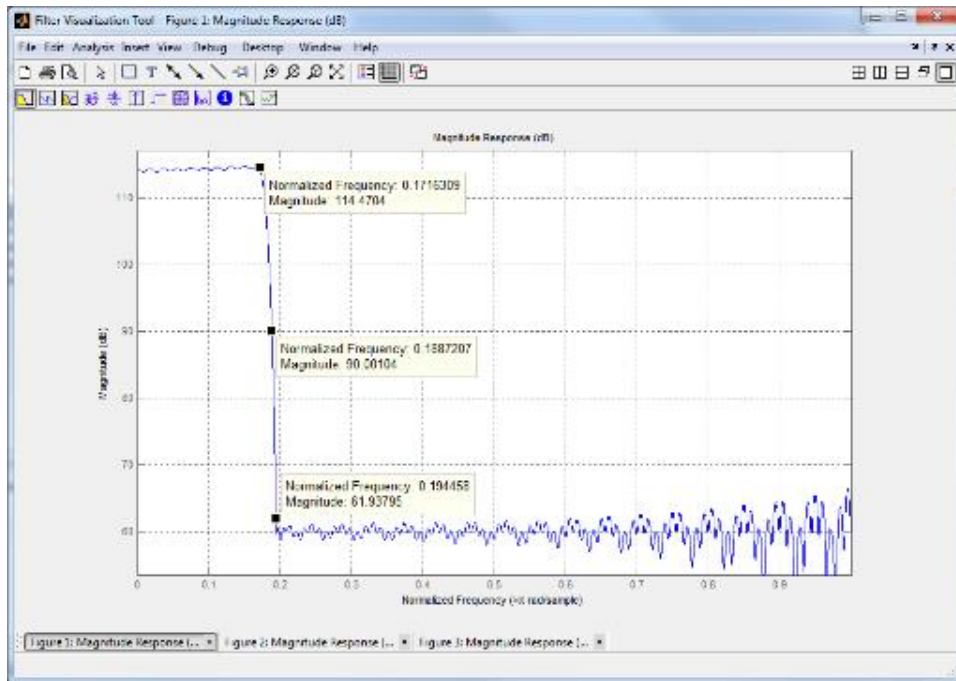

Figure 7. Graphic of FIR filter

The mathematical model of quadrature demodulator [8] of FM signal (3) is implemented in Multisim package using the structure of flowchart as shown in Fig. 8. Graph of demodulator's output signal (upper curve) and after a LF filter (lower curve) is shown in fig. 9.

$$X(t) = -\frac{d}{dt}\arg\left(y_I'(t) + y_Q'(t)\right)$$
$$X(t) = -\frac{d}{dt}\operatorname{arctg}\frac{y_Q'(t)}{y_I'(t)}$$
$$X(t) = \frac{\frac{dy_I'}{dt}y_Q'(t) - \frac{dy_Q'}{dt}y_I'(t)}{y_I'^2(t) + y_Q'^2(t)} \tag{3}$$
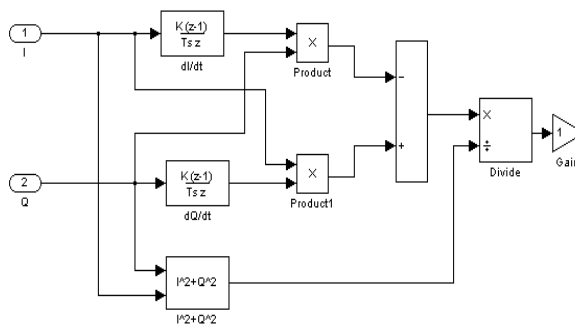
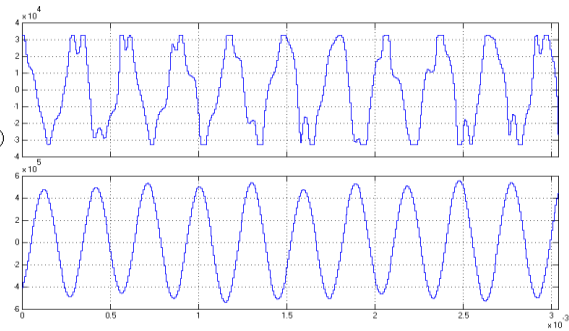**Figure 8.** A flowchart of quadrature demodulator

Figure 9. A graphic of demodulator's output signal (upper curve) and after LF filter (lower curve)

Experimental studies and practical results

According to the results of simulation modeling, a digital power control block has been developed and signal processing for digital VHF radio with a pseudo-random frequency hopping (FHSS mode) has being tested in JSC Ternopil radio factory Orion [9, 10]. The algorithm and software for the digital signal processor TMS320VC5502 of Texas Instrument Company, used in radios with FHSS mode to process the signal was developed. The view of a control block and digital signal processing is shown in Fig. 10.

Figure 10. The control block and digital signal processing, and a view of the radio station with FHSS

To test the adequacy and effectiveness of the simulation model and effectiveness of filter parameter selection are made by measuring the sensitivity of radio SINAD (signal to noise and distortion), which is widely used for analog and digital radio communication systems. SINAD [11, 12] is the ratio of rms signal amplitude to the mean root of the sum of squares (RSS) of all other spectral components, including harmonics. Non-lineal distortion of the measured signal is no higher than 25% and corresponds to the signal-to-noise ratio SINAD $(S + N) / N = 12$dB according to p. 4.8.16 State Standards of Ukraine 4184: 2003 [13].

The received results of measurement sensitivity for the working frequency range of the radio station are shown in Fig. 11. R.s.s.(root sum square) sensitivity of the receiver is 0.46 mV or -114 dBm with 12 dB SINAD, as shown in Fig. 11.
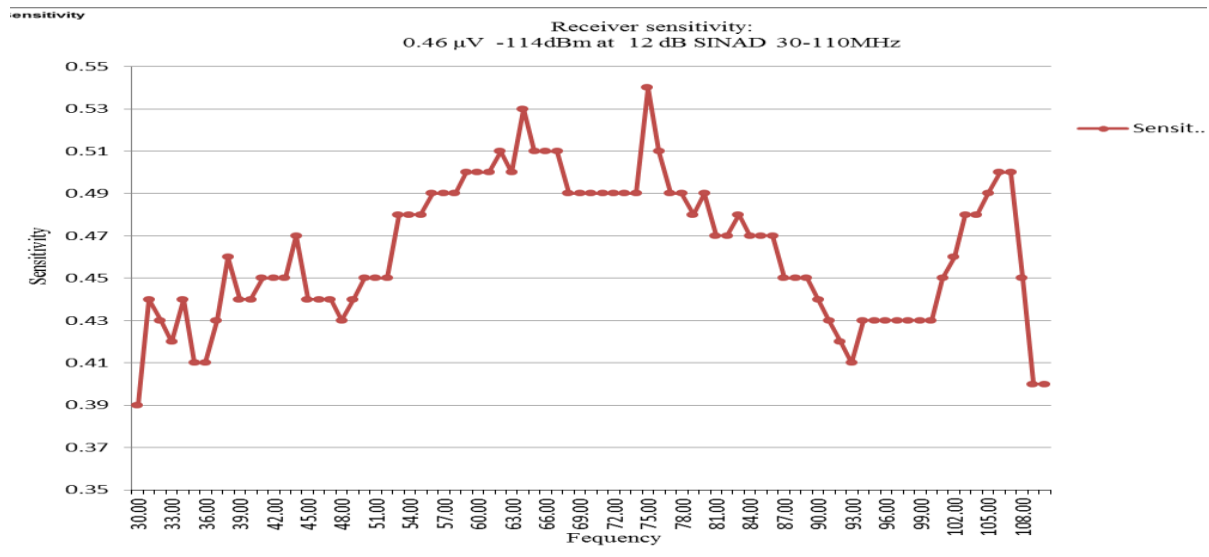
Figure 11. Receiver sensitivity

Conclusions. A model of communication channel with used digital receiver based on DDC AD6620 quadrature demodulator and FM signal at the signal processor DSP is represented. It was performed a simulation modeling of calculated filters DDC AD6620 quadrature demodulator and FM signals. According to the results of simulation modeling, it was developed the algorithm and software for TMS320VC5502 digital signal processor for processing radio signals with FHSS mode. The calculation of digital filters of DDC AD6620 was carried out.

As shown by experimental studies, using DDC for digital receivers allowed to raise receiver sensitivity in 16 dBm, from − 98 dBm up to − 114 dBm or in 2.45 mV, from to 2.9 mV up to 0.45 mV comparing to the receiver with the analog filtering channel. Also using a digital receiver based on DDC allowed to increase the degree of system integration and to reduce power consumption. Moving the main signal filtering from the analog to the digital field can reduce the requirements for analog signal filtering and flexibly tune a bandwidth of the receiver and improve technical features of radio generally.

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СИНТЕЗ ЦИФРОВОГО РАДІОПРИЙМАЧА ДЛЯ СИСТЕМИ ЗАХИЩЕНОГО ЗВ'ЯЗКУ ІЗ ПСЕВДОВИПАДКОВИМ ПЕРЕНАЛАШТУВАННЯМ РОБОЧОЇ ЧАСТОТИ

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Резюме. Наведено результати синтезу й моделювання роботи цифрового приймача на основі цифрового перетворювача частоти (DDC, Digital Down Converter) та цифрового сигнального процесора (DSP), що використовуються для опрацювання вхідних сигналів. Розглянуто спосіб побудови вузькосмугового приймача із цифровою фільтрацією, демодуляцією та опрацюванням сигналів. Наведено результати його використання у цифровій радіостанції з псевдовипадковим переналаштуванням робочої частоти (ППРЧ).

Ключові слова: псевдовипадкове переналаштування робочої частоти (ППРЧ), цифровий приймач, сигнальний процесор DSP, Digital Down Converter (DDC), квадратурний демодулятор, частотна модуляція (ЧМ).