CONSTRUCTION AND RESEARCH OF REVERSE FREQUENCY DIVIDERS

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Abstract: In the work, the reversible schemes of frequency dividers are constructed based on JK triggers are offered. It is proved that reversible frequency dividers work with insignificant differences in forward and reverse inclusions. When studying the frequency divider with direct inclusion, it was found that its real frequency differs from the calculated by 1.87%. And at return inclusion frequency dividers from are calculated on 2,17%. In general, such a relative error cannot be caused by the inaccuracy of the marker placement in the Multisim virtual oscilloscope. Such reversible frequency dividers can be used in unidirectional automated systems to build neural networks. **Keywords:** frequency divider, chichby module, division factor, trigger, counter.

1. Introduction

Appropriate electronic components must be used to receive, synchronize, decode and recognize high-speed data streams in real time [1]. The solution of these problems largely depends on the availability of high-quality synchronization signal generation systems produced by frequency dividers. Whether you need one (less) than the frequency of the master oscillator or a "grid" of interconnected frequencies, division by integer or fractional number, the basis of frequency dividers are always counters or registers with appropriate links between bits. In neural networks, this question becomes even more relevant because most of the problems that arise in information systems are poorly formalized and difficult to predict based on traditional mathematical methods. Each component of the information system can have its own reliability factor, which leads to a large amount of input information and a cumbersome solution [1-4].

The main parameters of the dividers are the division factor, speed, and complexity. When using frequency dividers to build neural networks, there is a need for their reversible use. They must work the same, both at the entrance and at the exit, depending on the mode of operation. Since these parameters are influenced directly by the organization of the circuitry of the device, the choice, and adoption of effective and original circuit solutions is an urgent task. The urgency of the problem has also increased because today for the creation of digital systems widely used chips programmable logic arrays (FPGA). If you do not specify a specific circuit solution, the means of the design package implements the node efficiently and optimally, but trivially, regardless of the method or language of description. This implementation will yield the original solution. With the neural network paradigm applying, it is possible to create parallel and distributed structures with high computing speed and greater efficiency to implement control tasks and ensure the reliability of information systems [1-3].

The obvious trend in the development of frequency dividers is to increase the range of their operating frequencies, performance, and usability in neural networks. Modern radio frequency applications, such as wireless personal and short-range LANs and car radars, make extensive use of millimetre-wave ranges. In addition, promising communication standards are being developed to service new applications, such as cellular communications and wireless data transmission in several new bands, including 28, 36, 45, 73, and 79 GHz.

To organize the divider (counter) with an arbitrary coefficient of division (conversion) using different methods [4]:

- exclusion of unnecessary states;
- use of feedback; - use of multiple modules;
- compulsory accrual (compulsory installation in 1 separate digit);
- reversible connection of digits.

This paper uses the feedback method, which gives less frequency division error.

Important components in radio equipment are frequency synthesizers with a wide range of tuning, high resolution, low cost, and low power consumption, so their technical implementation is of great interest to professionals.

2. Features of construction of reversible frequency dividers

A frequency divider is a counter with an arbitrary module M_0, which is covered by feedback with two triggers. The first trigger doubles the module, and the latter adds one, so in General, the module of such a counter is $D = 2 * M_0 + 1$. In this work, the frequency divider is built according to the scheme shown in Figure 1, *a*. To obtain the division of the frequency by an even number, you need to apply the input clock signal only to the first trigger, which multiplies the result by 2 (Fig. 1, *b*) [5-7].

Reversibility in the operation of frequency dividers allows you equivalently process the signal through these devices in the direction from input to output and in the opposite direction, i.e. the inputs and outputs of reversible

devices are inverted. The study of the operation of frequency dividers in the reverse mode is to build a switching circuit that allows the signal to flow, both in the forward and reverse directions. To do this, you need to provide a large input resistance at the input of the frequency divider: more than 50 kO and a load resistance of the order of several hundred kilohms. The output resistance, to avoid a decrease in the level of the output signal, must correspond to the ratio [8-11]:

$$R_{in} \geq 2R_{out} \tag{1}$$

where Rin and Rout – input and output pair of reversible frequency divider.

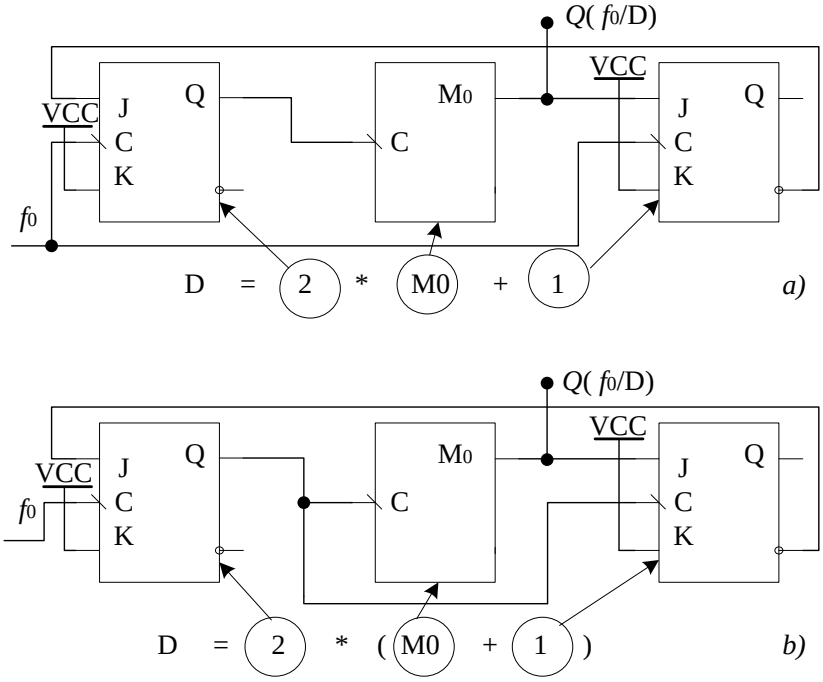

Fig. 1 Typical scheme of the frequency divider: *a*) for an odd number; *b*) on an even number

To ensure minimal amplitude-frequency distortion of the output signals, the circuit of the frequency dividers must be symmetrical, both in input and in output. At such inclusion, frequency dividers will work equally both indirect inclusion and in return (Fig. 2). When a signal source (IN) is connected to terminal ***b***, the load to terminal ***a*** of the logic element will operate in direct connection (input on the left and output on the right). When a signal source (IN) is connected to pin ***a***, the load on pin ***b*** of the logic element will operate in reverse (input on the right and output on the left).

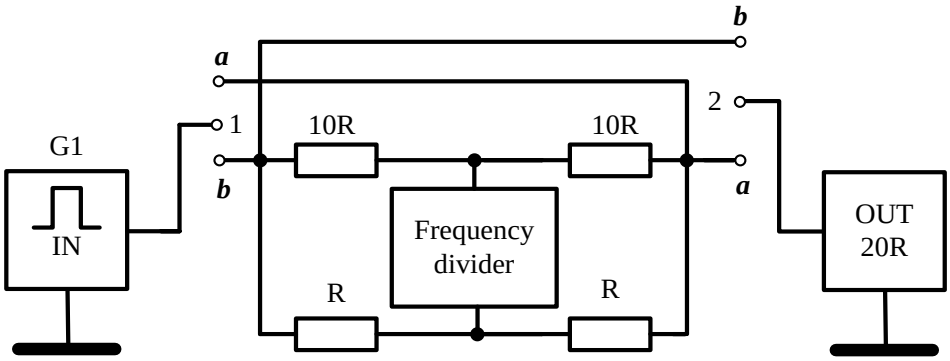

Fig. 2 Frequency divider switching scheme

Based on the general scheme shown in Fig. 2, we construct the scheme of the simple frequency divider with by 2 (Fig. 3). This version of the scheme allows using one trigger in reverse mode to divide the frequency by 2.

A resistive divider (R-10R) and the ratio of the input resistance of the signal source and the output load resistance, according to formula 1, provide the reversibility of the circuit (Fig. 3).

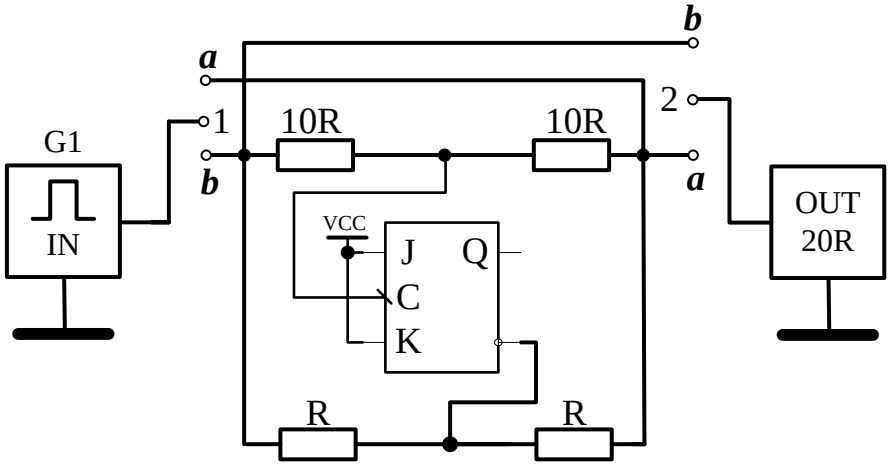

Fig. 3 Scheme of a simple frequency divider based on a JK-flip-flop

Devices are often needed that can divide the frequency by any number, not just 2, so the construction and simulation of the frequency divider circuit by 45 will be carried out further.

3. Simulation of the frequency divider in Multisim

Figure 4 shows a diagram of the study of the frequency divider by 45 in reverse mode. The circuit consists of: a rectangular signal generator G1 with a frequency of 45 kHz and a voltage of 5V; resistors R1 and R3 to provide high input resistance [11]; resistors R2 and R4 to provide output decoupling (matching output resistances); load resistance R5 (signal receiver); switches SA1 and SA2, which act as controllers, determining the input and output of the reversible frequency divider, in this case, the divider by 45.

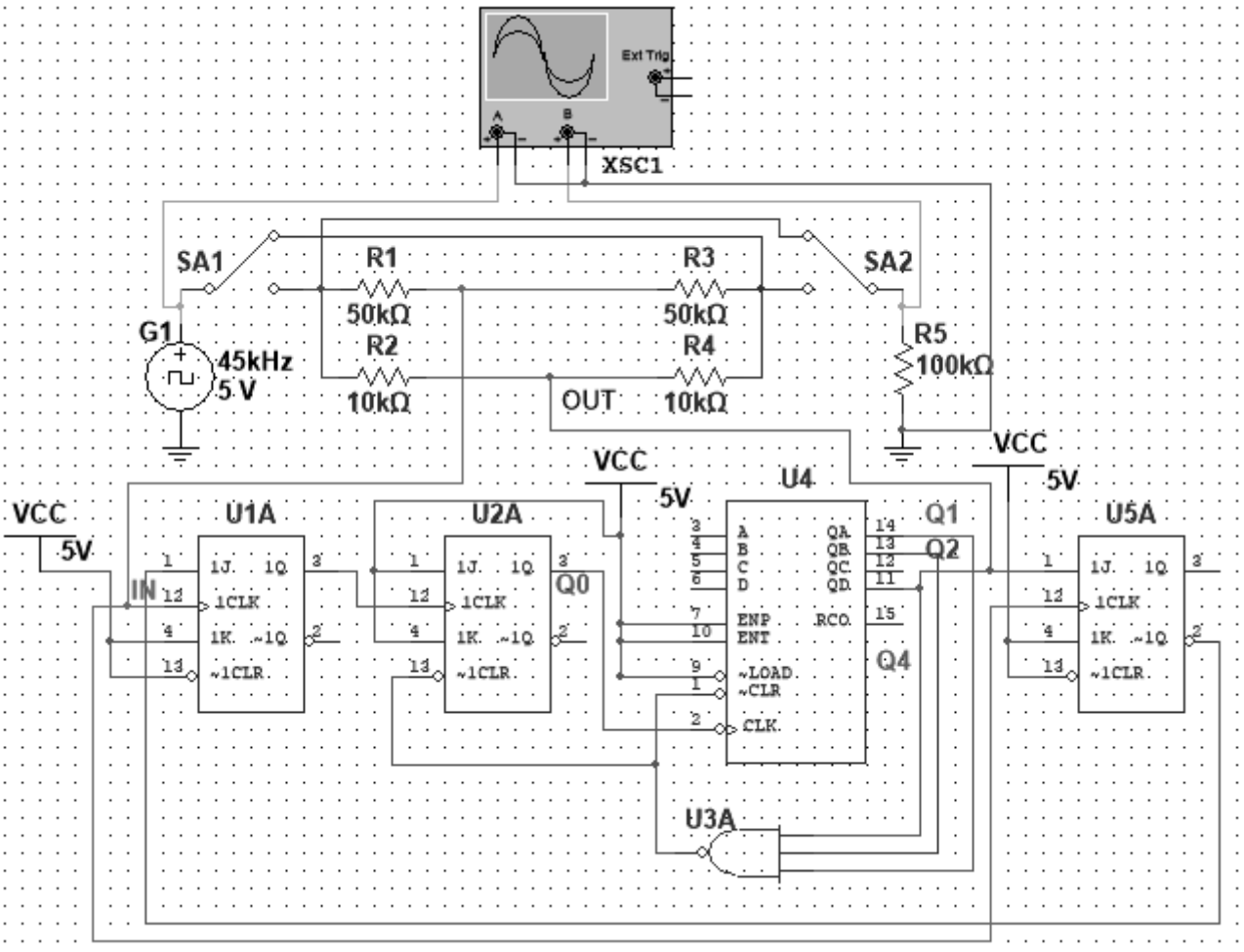

Fig. 4 Scheme of a frequency divider by 45 based on three JK-flip-flops, 4-digit counter and logical element NAND-3

The frequency divider based on: the counter (chips 74107N (U2A) and 74AS161N (U4)); trigger that multiplies the result of the counter by 2 (chip 74107N (U1A)); trigger, which adds to the result 1 (chip 74107N (U5A)) and the feedback element (chip 7410N (U3A)).

Figure 5 shows the timing diagrams of the buffer indirect inclusion, which show that such a frequency divider by 45 repeats the input signal without significant distortion.

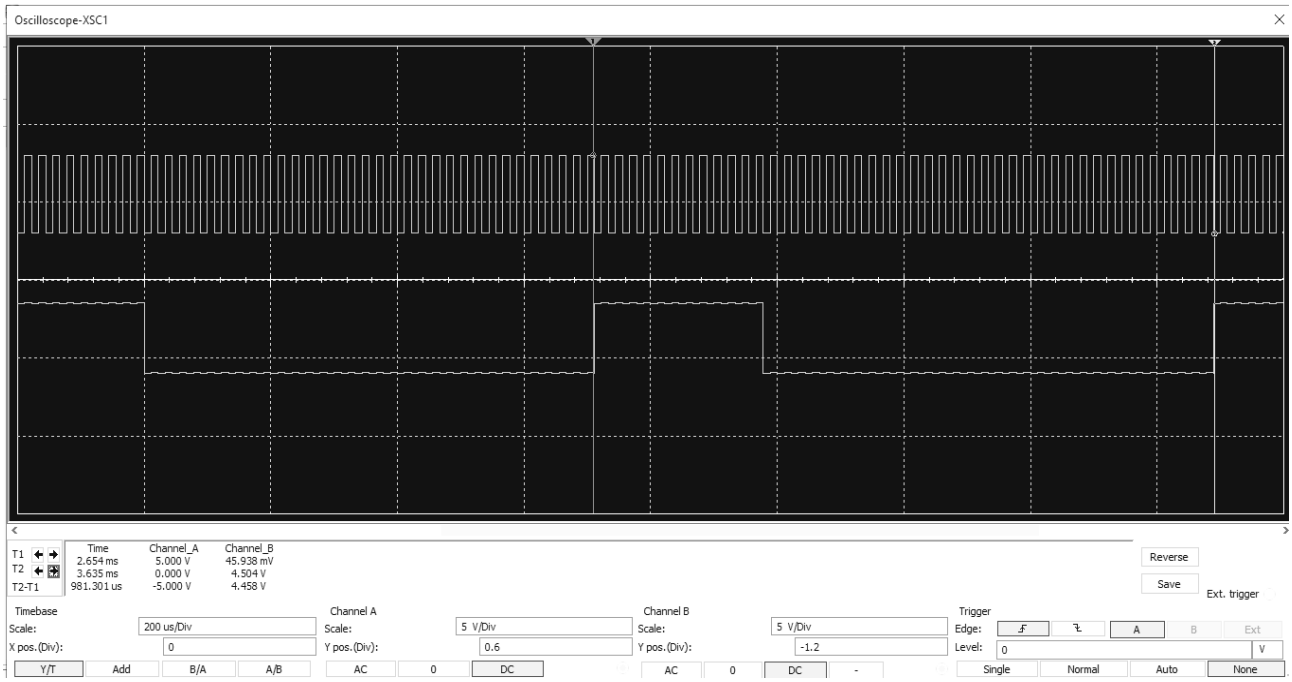

Fig. 5 The Oscillograms of the frequency divider by 45 in the direct-on mode

To conduct a study of the frequency divider in the reverse inclusion, you need to turn the switches SA1 and SA2 in the opposite position, as shown in Fig. 6. With this inclusion, the input became the output, and the output became the input.

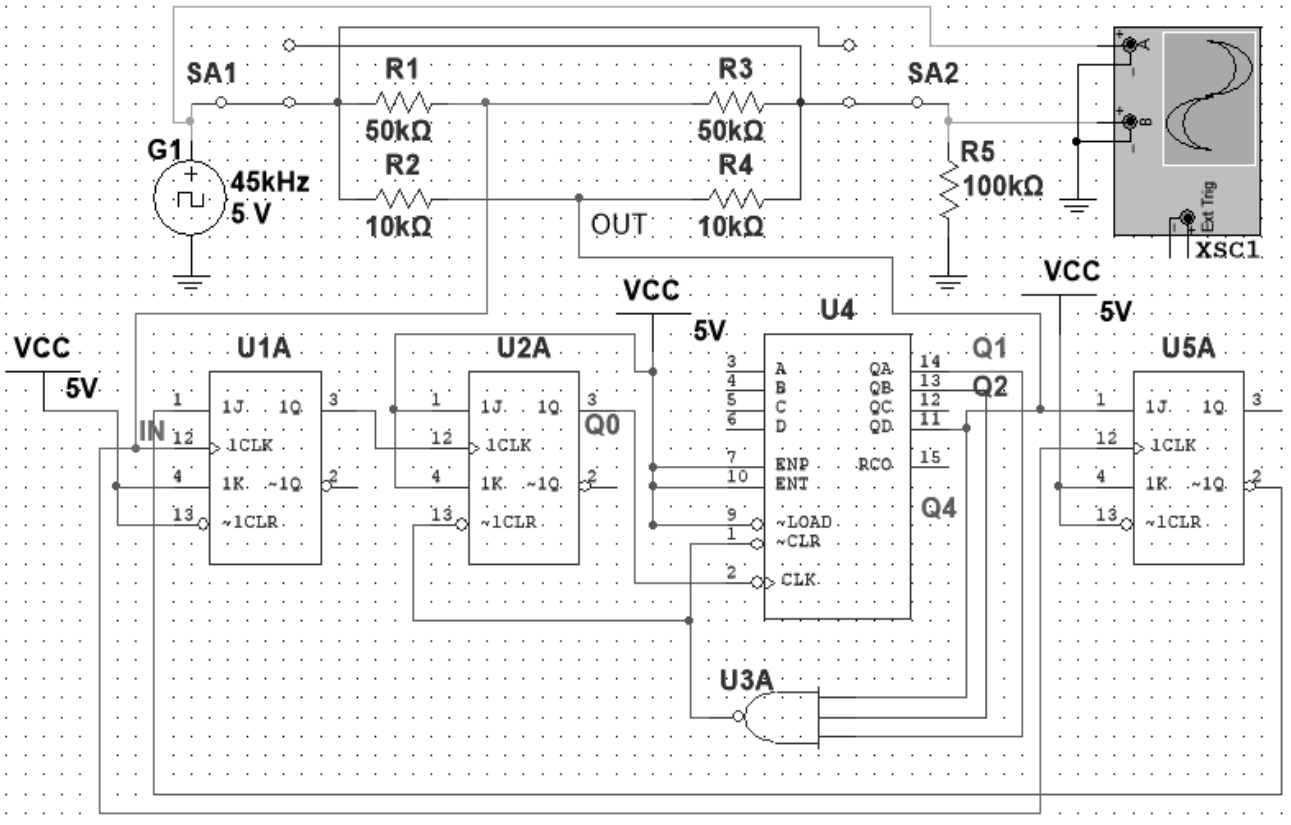

Fig. 6 Scheme of a frequency divider by 45 in reverse inclusion

By the simulation (Fig. 5) and the obtained oscillograms of the output signal, when directly connected, we calculate the frequency f_{out1} of the output signal and determine its relative error $\varepsilon_{out(1)}$. The measured period is equal to T_1 = 981.301 *us*.

$$f_{out1} = \frac{1}{T_1} = \frac{1}{981.301 \cdot 10^{-6}} = 1019,05 Hz;$$

$$\varepsilon_{out(1)} = \frac{|f_{out} - f_{out1}|}{f_{out1}} \cdot 100\% = \frac{1000 - 1019,05}{1019,05} \cdot 100\% = 1.87\%,$$

where f_{out} = 45000/45 = 1000 *Hz* – theoretical value of the output frequency of the divider, f_{out1} – the measured value of the frequency at the output of the divider in the direct-on mode.

The results of the study of the frequency divider in the inverse mode are shown in Figure 7. The measured period is equal to T_2 = 978.310 *us*.

By the simulation and the obtained oscillograms of the output signal, when directly connected, we calculate the frequency f_{out2} of the output signal and determine its relative error $\varepsilon_{out(2)}$.

$$f_{out1} = \frac{1}{T_2} = \frac{1}{978.310 \cdot 10^{-6}} = 1022,17 Hz;$$

$$out(2) = \frac{|f_{out} - f_{out2}|}{f_{out2}} \cdot 100\% = \frac{1000 - 1022,17}{1022,17} \cdot 100\% = 2.17\%,$$

where f_{out2} – the measured value of the frequency at the output of the divider in reverse inclusion.

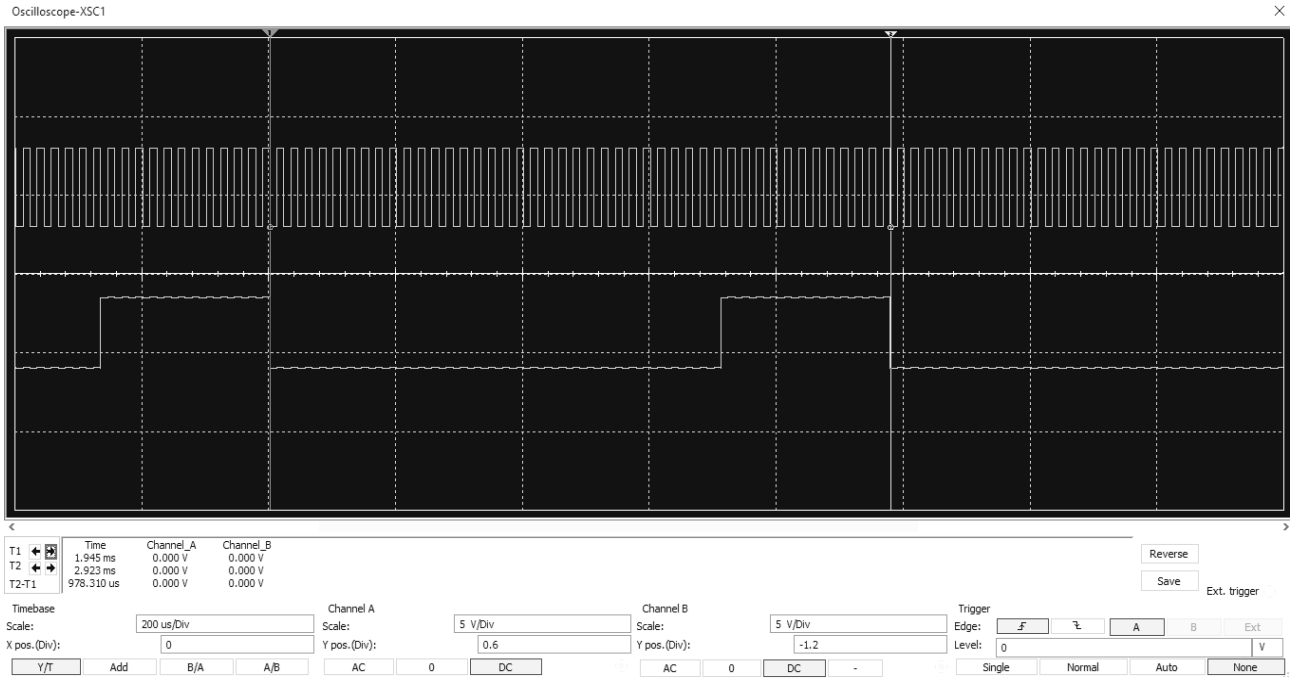

Fig. 7 The Oscillograms of the frequency divider by 45 in reverse inclusion

Modeling of the frequency divider with a division factor of 45 in the direct and reverse inclusion showed that the frequency deviation from the theoretical differs in the direct inclusion by 1.87%, and in the reverse by 2.17%.

The circuit of the reversible frequency divider is limited to a maximum frequency of 180 MHz. The frequency deviation will decrease as the division factor decreases and will increase as the division factor increases. This dependence was determined experimentally in the Multisim simulator.

The power supply of frequency dividers operating in reverse mode can be carried out both in the usual way, from DC power supplies 5V, and one or more external pulse signal generators, by summing them, for example, adder and subsequent filtration filter [10-11]. Such a load will not affect the shape and amplitude of the signals of the digital

generators. Note that the diode-resistive circuit protection of the inputs and outputs of CMOS chips allows their operation in low-current modes without the use of its power supply when applying signals to the input(s) of the chip.

4. Conclusions

A study of the reversible operation of frequency dividers has shown that they can work equally in both direct and reverse inclusion. Thus indirect inclusion of the output signal is closer to the theoretical value. Although such values may be the result of the inaccurate setting of markers in the virtual oscilloscope. But in general, such a deviation will not greatly affect the result of frequency division and the possibility of using such dividers in neural networks to build artificial intelligence systems.

For such frequency dividers, there is no difference between input and output, the main thing is to ensure the ratio of resistance between the signal source and the load.

The main task of this work was to show in principle the possibility of using ordinary frequency dividers in reverse mode. Because of the simulation, it was proved that the frequency dividers could work in reverse mode, using a special circuit of frequency synthesizers.

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